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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/733,659

12/11/2003

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RSW920030246US1 (136)

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05/01/2007

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EXAMINER

PATEL, HETUL B

ART UNIT

PAPER NUMBER

2186

MAIL DATE

DELIVERY MODE

05/01/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.



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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/733,659
Filing Date: December 11, 2003
Appellant(s): CHASE ET AL.

MAILED

MAY 01 2007

Technology Center 2100

Scott D. Paul
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed February 21, 2007 appealing from the Office action mailed September 11, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Workloads: PolyMix-2; [http://polygraph.ircache.net/Workloads/PolyMix-2](http://polygraph.ircache.net/Workloads/PolyMix-2;);

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(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4-6, 11 and 14-16 are rejected under 35 U.S.C. 102(b) as being anticipated by the content of the web page

<http://polygraph.ircache.net/Workloads/PolyMix-2/> posted on 05/29/2001, hereinafter, WEB.

As per claim 1, WEB discloses results of the workload “polymix-2” with a simple diagram showing a four-day trace of proxy load. WEB further discloses a table (on page 4 of 8) with different hit ratios (i.e. hit rates) determined in response to (different) given cache size(s) and the trace (i.e. in “Unif” column). WEB also computes the Zipf alpha coefficient for (different) given cache size(s), trace footprint and hit rate (i.e. “Zipf(0.2)”, “Zipf(0.4)” and “Zipf(0.6)” columns). The steps of selecting an optimal hit rate and computing an optimal cache size are inherent in the WEB disclosure because from the table, for any given/selected “optimal” hit rate/ratio, the optimal cache size is calculated as shown in the “cache size” column. For example, if the selected hit rate/ratio is 8.5, then the optimal cache size for that selected hit rate is 10.

As per claim 4, WEB teaches the claimed invention as described above and furthermore, WEB teaches that said determining step comprises parsing a log of server activity (i.e. recording how many hits for a given amount of time and requests) to identify said hit rate (e.g. see table on page 4 of 8).

As per claims 5 and 6, WEB teaches the claimed invention as described above and furthermore, WEB teaches that said identifying step comprises the step of identifying a current cache size (i.e. the cache size column in the table on page 4 of 8) and a contemporaneously experienced trace footprint (i.e. trace value) for a single content delivery server (i.e. for any one specific robot or server) and for a cluster of servers (i.e. for each robot or server) (e.g. see under "6.1 Allocation scheme" title on page 6 of 8).

As per claims 11 and 14-16, see arguments with respect to the rejection of claims 1 and 4-6, respectively. Claims 11 and 14-16 are also rejected based on the same rationale as the rejection of claims 1 and 4-6, respectively.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 2, 7-8 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over WEB.

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As per claim 2, WEB teaches the claimed invention as described above, but WEB does not clearly disclose about reconfiguring the cache memory allocation based upon said optimal cache size. However, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to reconfigure the cache memory allocation based upon said optimal cache size to achieve the desired/selected hit rate.

As per claim 7-8, WEB teaches the method for first computing Zipf alpha coefficient for current cache size, trace footprint and cache hit rate, and then, computing the optimal cache size based on the selected hit rate as described above in the rejection of claim 1, but does not clearly disclose about having a processor for computing Zipf alpha coefficient, a processor for computing optimal cache size and a sever log storing statistics. However, it would have been obvious to one of ordinary skill in the art at the time of the current invention was made to implement this method/model steps taught by WEB into a system and connect it via a communicative link as claimed so the system can be used to calculate the optimum cache size for one or more server(s) without running the software simulation.

As per claim 12, see arguments with respect to the rejection of claim 2. Claim 12 is also rejected based on the same rationale as the rejection of claim 2.

(10) Response to Argument

Appellant's argument:

- A.** The rejection of claims 1, 4-6, 11 and 14-16 under 35 USC 102 for anticipation based upon PolyMix
- A-1.** Claims 1 and 11 each recite a "current cache size" and a "contemporaneously experienced trace footprint". The Examiner's statement of the rejection only addresses a "cache size" and "a trace" without any mention that the cache size is current or that the trace footprint is contemporaneously experienced.
- A-2.** For an element to be inherently disclosed, the missing features must necessarily be present. The Examiner, however, has not establish that these missing features could be disclosed by PolyMix. Therefore, Appellants maintain their prior argument that PolyMix fails to identically disclose, either explicitly or inherently, all of the claimed limitations.
- B.** The rejection of claims 2, 7-8 and 12 under 35 USC 103 for obviousness based upon PolyMix
- B-1.** Nowhere has the Examiner pointed to any teachings or suggestions that the simulation model taught by PolyMix can be employed in the claimed system.

Examiner's response:

In response to Appellant's argument **A**, the rejection of claims 1, 4-6, 11 and 14-16 under 35 USC 102 for anticipation based upon PolyMix is *proper* because of the response to the Appellant's arguments **A-1** to **A-2** as shown below.

In response to Appellant's argument **A-1**, Examiner would like to point out to Appellant that in the PolyMix prior art, the different cache sizes (i.e. shown in the "Cache Size" column of the table shown on page 4 of 8) and associated traces (i.e. in "Unif" column in the table shown on page 4 of 8) were current at the time when it was generated. Therefore, each of the cache sizes in the "Cache Size" column are considered current cache size while they were generated and associated traces are considered as contemporaneously experienced. Hence, the PolyMix prior art does anticipate claims 1 and 11.

In response to Appellant's argument **A-2**, as clearly explained in the 'Remarks' section of the Final Office Action, the "current cache size" and "contemporaneously experienced trace footprint" are inherently taught by the PolyMix prior art because they can be easily derived from (i) the table shown on page 4 of 8 of the PolyMix prior art, and/or (ii) the graph (submitted with the Final Office Action) of the PolyMix prior art. If the "current cache size" and "contemporaneously experienced trace footprint" were clearly shown in either the table or graph of PolyMix, then they were considered as explicitly instead of inherently taught by the PolyMix prior art.

In response to Appellant's argument **B**, the rejection of claims 2, 7-8 and 12 under 35 USC 103 for obviousness based upon PolyMix is *proper* because of the response to the Appellant's argument **B-1** as shown below.

In response to Appellant's argument **B-1**, Examiner would like to point out to Appellant that it was so well known at the time of the current invention was made to employ the simulation model taught by the PolyMix prior art in the claimed system. Examiner

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should have, in the last (Final) office action, taken the Official Notice for this claimed feature to be well known in the art, however, examiner assumed that the implementation of a simulation model into a system is notoriously old in the art and did not expect to get challenged on this subject matter.

(11) Related Proceeding(s) Appendix


No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.


Respectfully submitted,

H. B. Patel 04/25/2007
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Patent Examiner
Art Unit 2186

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